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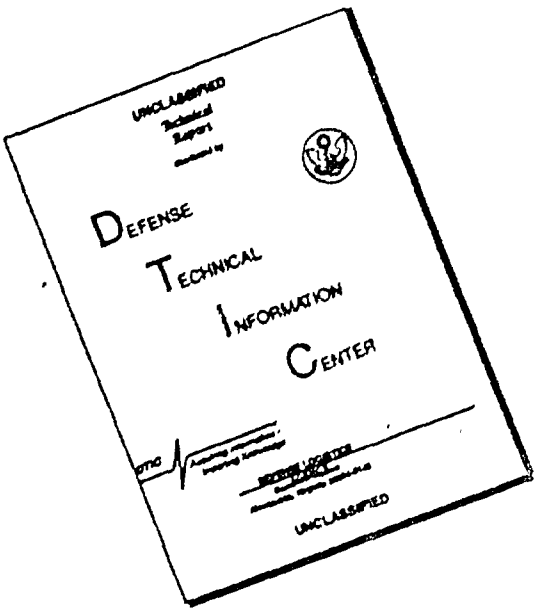


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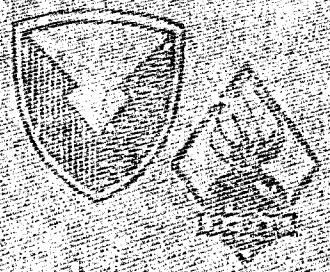
HDL-TR-2170
February 1990



# Evaluating a HEMP-Hardened Signal Entry TPD Enclosure

by Robert Atkinson
Raymond E. Parsons, Jr.
Rudolph Prushnzka





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19. ABSTRACT (*Continue on reverse if necessary and identify by block number*)

Working within the sponsorship and authority of the Naval Electronics Engineering Activity, Pacific (NEEACT PAC), personnel of the Harry Diamond Laboratories (HDL) evaluated the performance of a prototype signal entrance enclosure exposed to transient signals related to high-altitude electromagnetic pulse (HEMP). This report discusses the prototype enclosure design, supporting laboratory experiments, and data analysis, such as (1) shielding effectiveness, (2) degree of transient suppression as provided by internal terminal protection device (TPD) circuits, (3) response to high transient current levels, and (4) discrepancies and methods for improvements.

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# 1. Introduction

Working within the sponsorship and authority of the Naval Electronics Engineering Activity, Pacific (NEEACT PAC), personnel of the Harry Diamond Laboratories (HDL) assessed the hardening capabilities of a prototype signal entrance enclosure as well as of prototype terminal protection devices (TPD's). As the Army's lead laboratory for evaluating the effects of high-altitude electromagnetic pulse (HEMP), HDL is frequently called on for its technical expertise in systems nuclear survivability. Since the effects of a HEMP event can be devastating to communications, they must be minimized either by shielding data lines from the excessive electromagnetic fields or by suppressing the characteristically large induced currents and voltages.

HDL has developed this technology from designing and evaluating prototypical TPD hardware and developing circuit architectures. Since then, many of the prototype TPD's have reached the private sector, and circuit specifications and constructs are now standard practice. Today, second- and third-generation components, combined with new circuit architectures, are developed for specific requirements and must be evaluated for HEMP hardness.

The principal concerns for the effort reported are as follows:

a. To assess the enclosure's ability to shield the internal TPD circuits from HEMP-related radiation.

b. To determine the degree of transient suppression provided by the TPD's.

c. To assess TPD circuit architecture response to large currents.

d. To determine areas of weakness and methods of improvement.

The basic TPD circuit addressed in this report is a two-stage device. The first stage of the TPD circuit is a gas-filled high-energy suppressor, also known as a "spark gap" or "gas tube." The second stage, a low-energy suppressor, is a TransZorb* (a fast-response, bipolar, Zener-type diode). A delay circuit consisting of an inductor and a resistor couples the two stages together. These components, manufactured by Siemens Industries (SI) and General Semiconductor Industries (GSI), are assembled on several printed circuit (PC) boards. The boards are

*TransZorb is a registered trademark of GSI.

modular and are housed within the signal entry enclosure. The signal entry enclosure is constructed from two Hoffman NEMA type-12 enclosure cabinets welded back to back. Circuit continuity from one enclosure to the other is through a filter pin connector. Wiring is terminated at a $10 \times 26$ terminal block inside the enclosure.

In the evaluation of the enclosure and TPD's, test efforts were extensive and every aspect was investigated. The evaluation included

a. measuring the shielding effectiveness (SE) of the TPD enclosure,

b. measuring individual TPD response to high-energy transient injection, and

c. measuring the end-to-end circuit response.

# 2. Recommendations

HDL recommends the following changes to the TPD enclosure's physical structure:

a. The hinged sides of the enclosure's doors are the major source of aperture leaks. Replacing the door's hinges with fastening bolts (similar to those on the other door sides) will reduce the extent of this leakage.

b. The amount of rf leakage can be minimized by applying uniform torque about the door gasket. A spring (part of the fastener assembly) regulates the amount of measurable torque and is susceptible to wear and deformation through constant pressure. Replacing this spring with one using a larger diameter wire with higher tensile strength will prevent spring distortion and increase spring life expectancy and performance.

c. Bolt pressure stays must be removed or modified. They regulate the amount of pressure applied to the door gasket, limiting the extent to which the tightening bolt can advance. A very slight increase in bolt length causes the bolt tip to bind with the stay, and any additional torque applied to the bolt shears the head. Removing the broken stud is very inconvenient.

The following recommendations are based upon results obtained from evaluating the individual TPD components:

a. The high-voltage board has a rated clamping voltage too close to that of the surge arrestor board. Either a surge arrestor with a higher breakdown voltage or a TransZorb with a lower clamping voltage must be selected.

b. The F-type connector impedes the action of the TPD circuitry on the slow-speed (40 kb/s) boards. Therefore, if no electromagnetic compatibility or TEMPEST requirements are to be met, the F-type connector should be used with only the GZ74416B high-voltage board.

The following recommendations are based upon results obtained from evaluating the TPD boards and associated electrical architecture:

a. HDL recommends that if the present PC board design is to be used, all hex head screws and rivets connecting the board to its individual chassis ground should be replaced with machine screws and lock washers.

b. HDL suggests that if the present circuit geometry (specifically, the first-stage board separated from the second-stage boards) is to be used, circuit response may improve if the spark-gap board is redesigned, fitted with three-element gas tubes, and etched with wider ground return leads.

   Only 50 percent of surge arrestor components will be needed. This will allow for a much larger area of the board to be occupied by the wider ground return leads. The board size will be physically reduced. This will result in cost savings and improved electrical performance in terms of spark-gap switching speed.

c. If the present circuit geometry can be changed, the first and second stages may be included together on a single PC board, or the wiring from the first stage (surge arrestor board) to the second stage (TransZorb boards) must be shortened. An alternative would be to have the manufacturer design the TPD circuits to specifications that will reduce the overshoot at the output.

d. All unused cables must be grounded in compartment 1 of the shielded enclosure. The unused cables that are grounded in compartment 2 unnecessarily carry currents into that compartment and add to the cross-coupling problems observed at the terminal block output.

   Furthermore, HEMP hardening of multiconductor cable suggests, at minimum, a double-shield construction. It is strongly recommended that the input cable interface be double-shielded cable with individual drain wire shields on each wire pair within the overall cable shield.

HDL recommends the following actions to ensure and extend life-cycle survivability for the TPD enclosure:

a. The radio frequency interference (RFI) gasket and mating surfaces must be inspected periodically to assure a paint-free surface and gasket uniformity.

b. The fastening bolts must be uniformly tightened using a staggered order to 12 to 15 ft-lb. Tightening by torque wrench is preferred over unregulated tightening by hand.

c. Periodic recertification, using an rf-sensitive test set, or "sniffer," must be implemented. Identification and subsequent replacement of degraded (permanently deformed) gaskets are essential for rf integrity.

# 3. Design Improvements

The suggestions in section 2, provided as engineering guidelines in support of a final design solution, are to aid the design engineers of the prototype enclosure by (1) suggesting alternative designs to reduce the present design inefficiencies, (2) providing information on alternative components, and (3) making recommendations based upon various documented installation architectures.

In accordance with the recommendation above, the following discussion assumes that double-shielded cables will be used to increase the cable transfer impedance of the TPD enclosure (shown in fig. 1). The fact that the cable bun[illegible] supplied for the evaluation efforts had only a single-layer shield was a noted design weakness.

Any enclosure that will be installed as an integral part of a larger electromagnetic volume shield is only effective to the extent that EMP transients on penetrators are controlled. These transients are con-

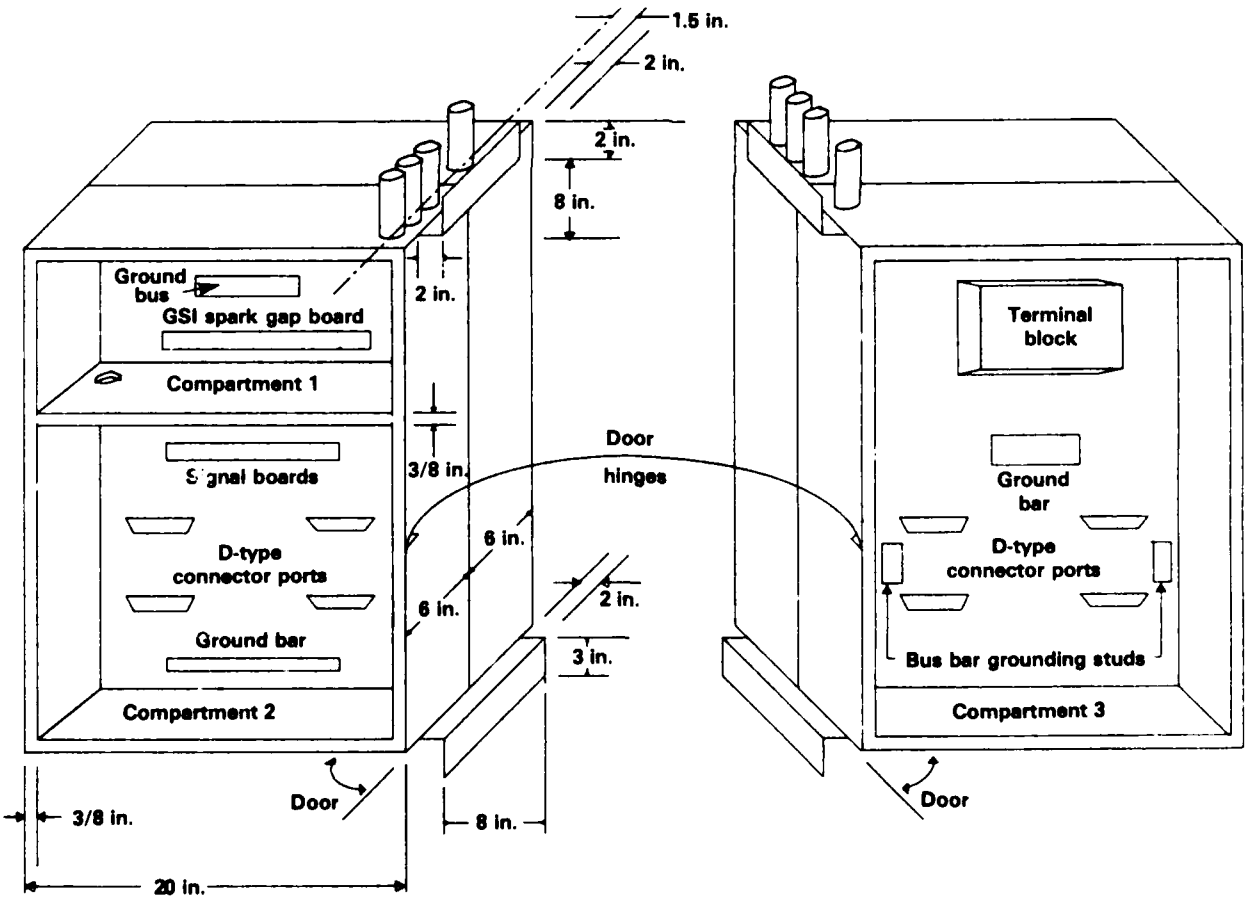



**Figure 1. Present enclosure design.**

trolled by ensuring that the conducting surface is continuous, to allow free flow of electrons over the whole surface of the enclosure shielding (outer) layer (the larger volume).

Generally, it is desirable that large currents be diverted away from the shielding surface as soon as possible. Therefore, if the TPD enclosure is to be part of a larger shielded facility and signal lines enter the TPD enclosure through the stuffing tubes, the cable bundle shield should be terminated on the exterior of the enclosure and not inside the stuffing tube. This is an inherent weakness of the present design.

All unused data wires should be connected to a single-point ground using the shortest possible path. Furthermore, there should be no electrical connection between the internal signal ground and the external shield ground.

Because of the "generic" application of this TPD enclosure, grounding schemes become complex. Engineering guidelines for grounding and shielding dictate specific consideration for each individual application. In any case, the integrity of the TPD enclosure/facility shield must be maintained.

Within the "dirty" (that is, input) side of the enclosure are two compartments. The first (compartment 1) holds the surge arrestor board (GZ74416A). The second (compartment 2) contains the TransZorb boards (GZ74416B, GZ74602B, and GZ74427A). The two compartments are separated by a steel bulkhead. The design intent of two separate compartments is to "bleed" energy from the surge arrestors and TransZorbs and to divert this energy to ground in the interior of the enclosure. However, to connect the boards, an aperture had to be cut in the bulkhead separating these two compartments—a design weakness.

A suggestion is to install feed-through connectors instead of the aperture on the bulkhead between the two compartments. This would maintain the shield integrity, provided that all unused data wires were grounded in compartment 1. The weakness in the present design is that unused data wires were grounded in compartment 2.

Another weakness in this brassboard design lies in the construction of the hinged doors. One way of improving the present design is shown in figure 2. Fastener positions are changed for closer spacing and are located on all four door sides. The hinge is removed.

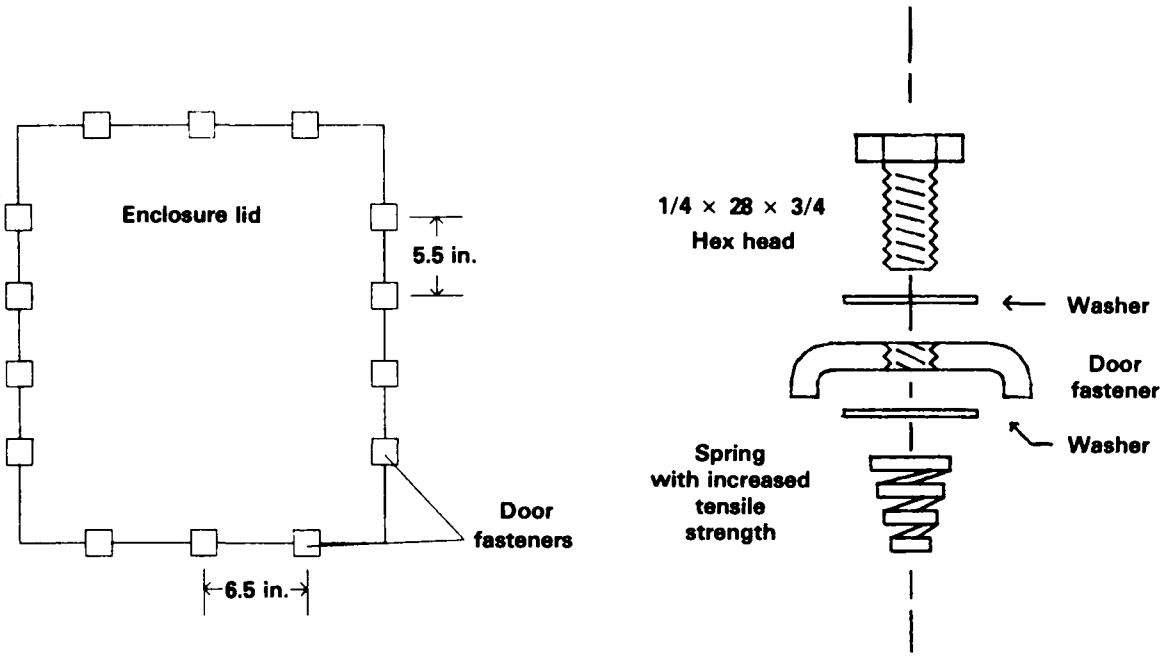



**Figure 2. Suggested enclosure door modifications.**

Sudden frequency instability often results from defects in either component manufacturing or mounting onto PC boards. Loose components or connections often give rise to frequency problems. These problems will occur when the screws around the edges of the PC board are used to connect the board to the chassis ground. Similarly, the soldered rivets make a fine connection to chassis ground when first assembled. Eventually, however, corrosion and looseness from mechanical weakening cause intermittent or high-impedance ground connections.

If rivets become loosened, the mounting screws should be moved and the rivets drilled out. Next the area of the PC board should be lightly sanded around the location of the screws and rivets. The board should be remounted to its ground chassis with machine screws, lockwashers, and nuts. The connections should be coated with lacquer to prevent corrosion.

Other changes to the structure should be made to reduce the physical size of the enclosure and the quantity of components used.

First, only a single Hoffman (or similar) enclosure should be used. The six modular components, which include the surge arrestor board, four TransZorb boards, and the terminal block, will easily fit into a single enclosure.

Second, the selection of the surge arrestor itself is a noted weakness in the system design. The surge arrestor breakdown voltage is too close to that of the clamping voltage level of the GZ74416B high-voltage board; this is a bad choice because it could lead to circuit malfunction.

Furthermore, the surge arrestor board is itself inefficient and could defeat the intentions for a modular design. Since all the surge arrestors are mounted on a single board requiring many soldered connections, it is necessary to replace the board when even a single device becomes damaged. Therefore, alternative schemes using the surge arrestors should be considered. One alternative might be to install self-contained and shielded surge arrestors in place of the surge arrestor board. The advantage is that one failed arrestor could easily be replaced without interrupting the rest of the circuits.

In an alternative design, shown in figure 3, F1537/G surge arrestors are mounted to the enclosure's case (shown in fig. 3b) in place of an arrestor board. (The F1537/G surge arrestor is further described in fig.

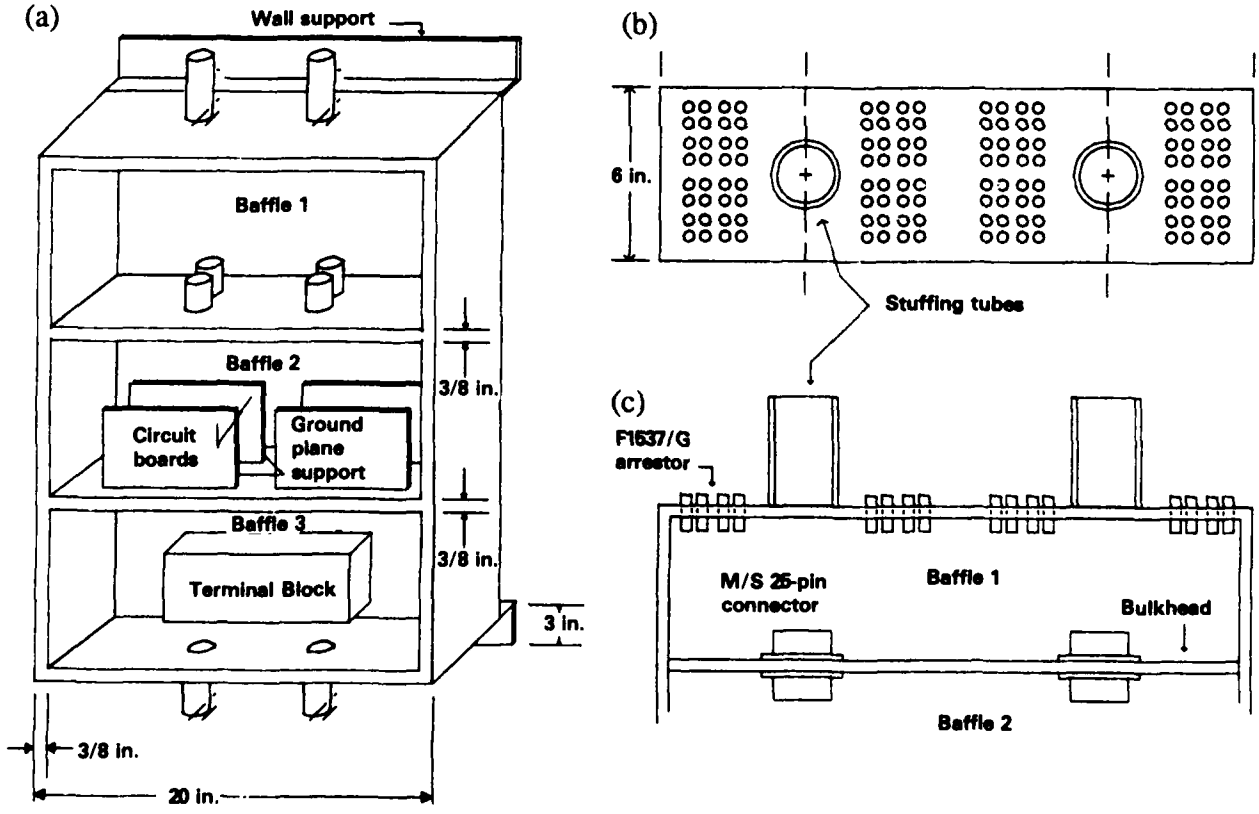



**Figure 3. Redesign recommendations: (a) front view, (b) top view, and (c) detail of front view.**

4.) M/S 25-pin connectors are mounted on the bulkhead separating the equivalent of compartments 1 and 2. Other 25-pin connectors (D-types) are located on the bulkhead separating the equivalent of compartments 2 and 3. The inside of the enclosure's door (not shown) has RFI gasket material installed to coincide with the bulkhead/shelf edges when the door is secured. Note: an F1538/G binding-post surge arrestor can be substituted for the F1537/G in special applications.

To reduce component quantity and cost and to increase performance and reliability, a three-element surge arrestor could replace the two-element 230-84PM arrestor presently used. An advantage to this is that fewer components (half as many) are required on the surge arrestor board. (An example of a TPD circuit employing such an arrestor is shown in fig. 5.) This approach reduces differential voltage between (data wire) surge arrestors. Figure 6 displays typical waveforms from the output of a three-element TPD and the effect of nonsimultaneous firing of the surge arrestors.

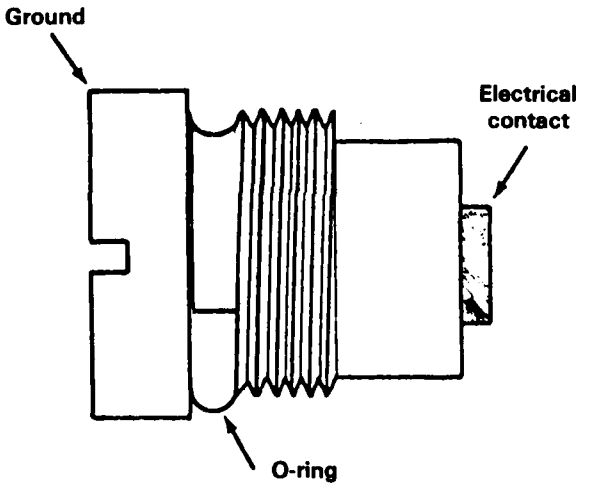



Figure 4. F1537/G surge arrestor.

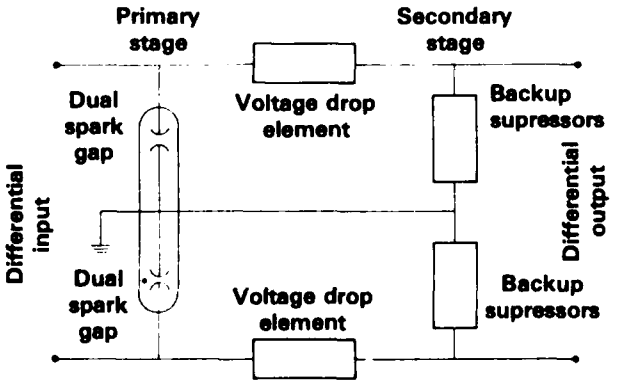



Figure 5. TPD circuit using a three-element spark gap.

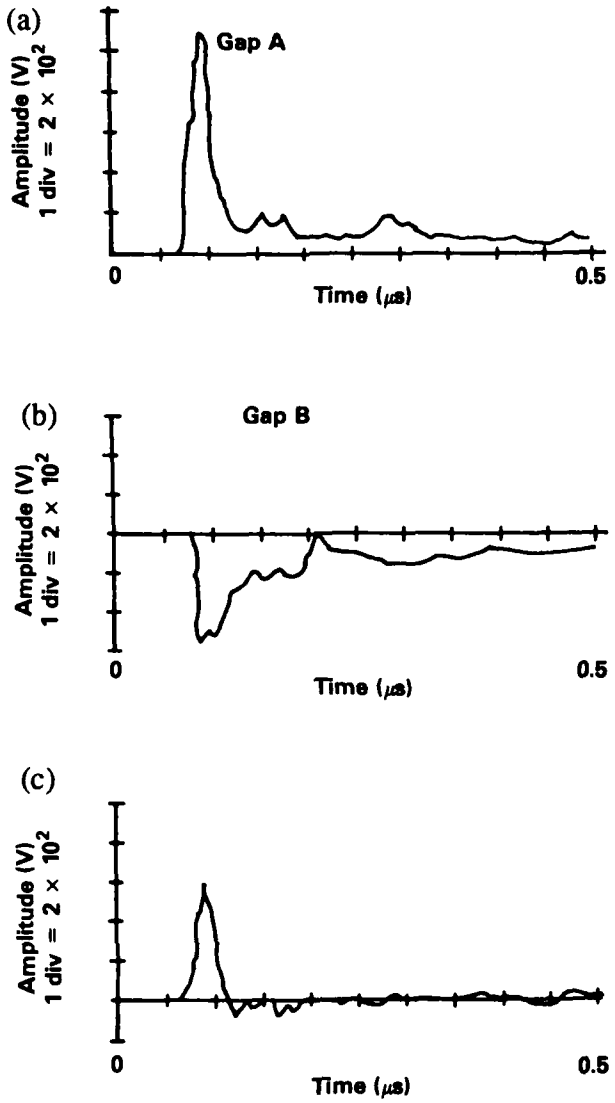



**Figure 6. Typical differential spark gap voltage: (a) slow sparking gap, showing overshoot, (b) normally sparking gap, inverted voltage, and (c) differential of gaps A and B.**

A final solution, and probably the most desirable, is to include the primary and secondary TPD stages onto a single circuit board. The requirement that the TPD circuits be modular is maintained, replacing damaged components is simplified, and periodic testing and certification of the component boards is comparatively easy.

A final consideration: the methods by which the final design is to be implemented and the systems that it will interface (leading both into and out of the enclosure) are equally important. Some of these have been addressed throughout this text, and others need be addressed when the design is completed and installation is imminent.

# 4. Shielding Effectiveness Evaluation

## 4.1 Summary

Several areas were investigated in the evaluation of the prototype TPD enclosure's SE: the baseline door fastener mechanical torque characteristics at frequencies within the lf, hf, vhf, and uhf bands, and general enclosure degradation.

Aperture leakage was determined for various door-fastener mechanical torques at 450 MHz: SE for the input (dirty) side of the box ranged from 45 dB at 2 ft-lb to 80 dB at 17.5 ft-lb of torque. SE for the output (clean) side of the box range from 69 dB at 1 ft-lb to 79 dB at 17.5 ft-lb of torque.

The best SE results were obtained when the enclosure's door fasteners were tightened between 12 and 15 ft-lb of torque.

SE for the input (dirty) side to the output (clean) side of the box was measured at 50 dB at 15 ft-lb of torque for both doors.

In another baseline aperture leakage characterization, the TPD enclosure was exposed to electric fields within a parallel-plate transmission line at selected frequencies ranging from 500 kHz up to and including 102 MHz. Within a frequency band extending from 25 to 100 MHz and with a torque of 15 ft-lb applied to each fastener, SE ranged from 51 to 116 dB for the clean compartment door and from 63 to 117 dB for the dirty compartment door.

Aperture leakage degradation was assessed by determining the effect of insufficient or unequal torque on door fasteners, over a period of time, and repeated opening and closing of the door.

## 4.2 Baseline SE

The purpose of this analysis was to determine the baseline shielding effectiveness of the TPD enclosure. Establishing a baseline allows us to make a quantitative examination of the condition of the door gaskets and gasket degradation due to multiple openings and closings of the enclosure's doors; it also lets us assess and correlate manufacturer's specifications for both the Hoffman enclosures and the Chromerics conductive gaskets.

Test protocol was based upon standard operating procedures using the TS-450 shielded enclosure test set: the test set's compactness permitted various configurations for SE analysis.

The tabulated data are shown in figures 7 to 9.

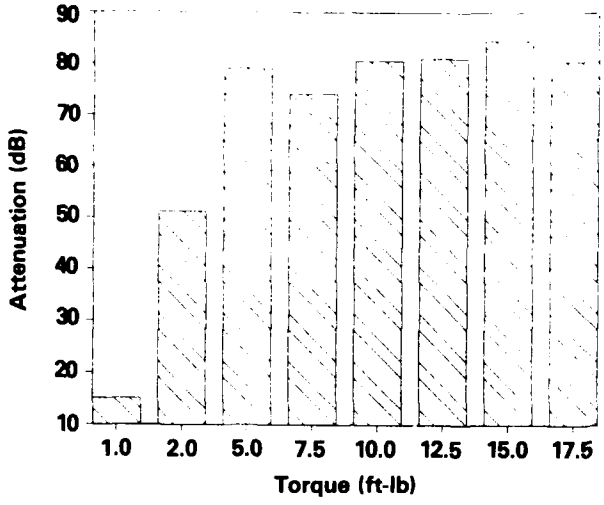



Figure 7. Compartment 1 (dirty side) baseline SE results.

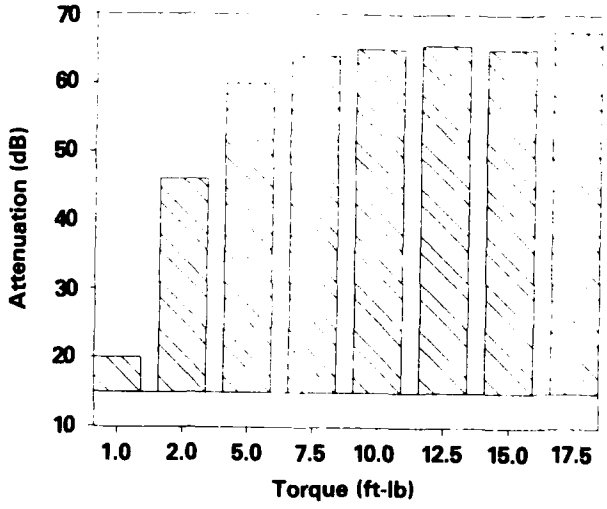



Figure 8. Compartment 2 (dirty side) baseline SE results.

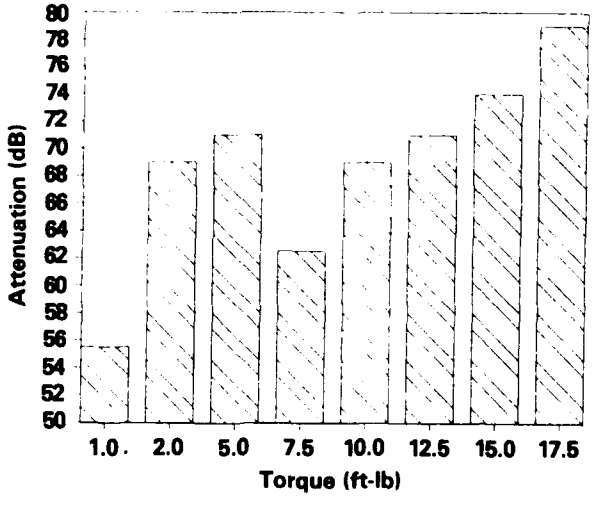



Figure 9. Compartment 3 (clean side) baseline SE results.

## 4.3 lf-uhf SE

For the assessment of the enclosure's SE at various frequencies, the enclosure was placed within a parallel-plate transmission line and exposed to low-level continuous wave (cw) fields. Using the baseline SE studies at 450 MHz as a guide, we oriented the enclosure so that the most susceptible part of the enclosure (the hinges) was positioned in the direction of the electric field.

Tables 1 and 2 indicate SE of the enclosure across the range of measurable frequencies, from 25 to 100 MHz. The maximum dynamic range of the measurement system (shown in fig. A-4, in the appendix) was 120 dB.

The clean compartment was more susceptible than the dirty compartment. One reason for this is as follows: The hinged side of the enclosure door demonstrated the greatest tendency to leak radiated signals into the adjacent compartment. If the mating connection is viewed as an aperture approximately 530 mm long with a relatively small associated width and thickness (perhaps 1 and 5 mm, respectively), we calculate that SE close to the aperture would range from about 46 dB at 25 MHz to about 34 dB at 100 MHz. For the dirty compartment, a metal plate was introduced to cut the aperture roughly in half. The resultant aperture is smaller, and SE across the frequency band increases.

**Table 1. Dirty compartment field levels**

| Frequency (MHz) | SE (dB) |
|---|---|
| 25.0 | 69 |
| 30.0 | 107 |
| 30.5 | 108 |
| 31.0 | 100 |
| 46.5 | 101 |
| 50.0 | 100 |
| 55.0 | 116 |
| 60.0 | 63 |
| 65.0 | 112 |
| 71.5 | 115 |
| 78.0 | 89 |
| 90.0 | 117 |
| 100.0 | 87 |

**Table 2. Clean compartment field levels**

| Frequency (MHz) | SE (dB) |
|---|---|
| 25.0 | 69 |
| 30.0 | 75 |
| 30.5 | 75 |
| 31.0 | 65 |
| 46.5 | 102 |
| 50.0 | 102 |
| 55.0 | 116 |
| 60.0 | 63 |
| 65.0 | 68 |
| 71.5 | 79 |
| 78.0 | 53 |
| 90.0 | 82 |
| 100.0 | 51 |

## 4.4 SE Degradation

One set of tests assessed the degradation in SE due to multiple openings and closings of the enclosure's doors. For this assessment, test methods, equipment, and procedures were the same as those described in section 4.2. Results are as shown in figures 10 to 12.

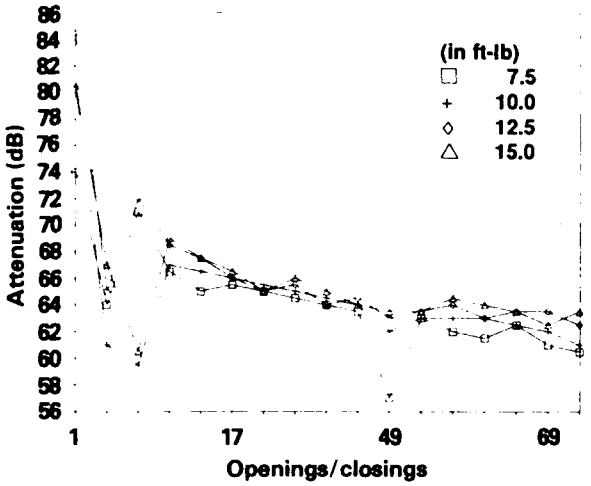



Figure 10. SE degradation curves for compartment 1 (dirty side).

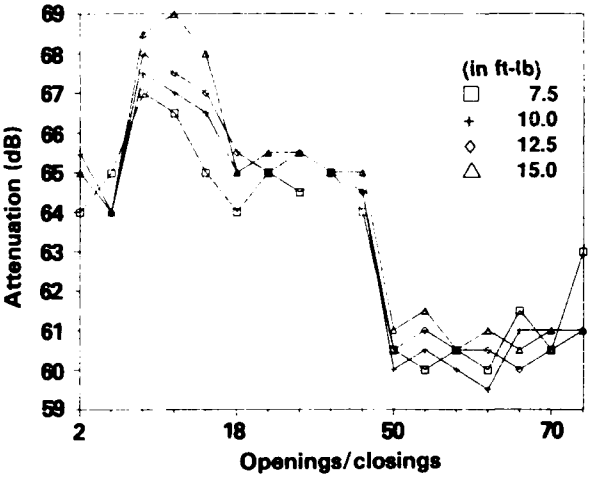



Figure 11. SE degradation curves for compartment 2 (dirty side).

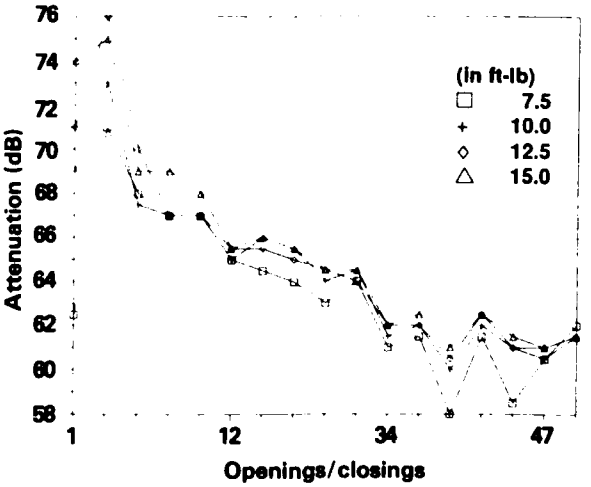



Figure 12. SE degradation curves for compartment 3 (clean side).

# 5. TPD Component Evaluation

## 5.1 Summary

We evaluated the performance of the individual TPD circuits and components (F-type connectors, surge arrestors, and TransZorb boards) in the presence of a HEMP double-exponential pulse relatable to the Quadripartite Standardization Agreement (QSTAG) and MIL-STD-2169 signatures. Components were evaluated to levels of stress relative to their physical and electrical location within the enclosure.

The components evaluated separately were surge arrestors, a 25-pin F-type connector, and PC boards (containing inductors, resistors, and TransZorbs). Generally, these components performed well and in most cases met the manufacturers' standards. Exceptions are noted.

The 25-pin F-type connector, when excited at approximately 400 V, was found to be extremely susceptible to pin-to-pin cross coupling during the transient and would therefore be inefficient in the present design. Differences in output signals were minimized by replacing the F-type connector with a D-type connector.

Typical clamping voltage levels for the 230-84PM surge arrestor, by itself, were found to be within manufacturer specifications.

When the 230-84PM was mounted near the PC board, the total TPD circuit (surge arrestor, PC board, and filter pin connector) performed reasonably well. Clamping voltages for the combined TPD circuits were very close to those stated by the manufacturer; however, the high-speed board (GZ74602B) consistently allowed voltage overshoots of nearly twice the intended clamping voltage.

The three PC boards were installed in the enclosure and successfully passed data at rates up to and including 32 kb/s.

## 5.2 F-Type Filter-Pin Connector

The 25-pin F-type connector was characterized for the following three features using a network analyzer and various HDL-designed pulsers: (1) conformity with manufacturer's specifications, (2) filter response to pulse injection, and (3) degradation in insertion loss due to pulse testing.

As can be observed from table 3, the measured insertion loss exceeded the values stated by the manufacturer at almost every frequency before pulse testing. Further, a degradation in the connector's insertion loss was observed after pulse testing was completed.

Measured results indicated that the filters were attenuating pulsed injection signals at the levels shown in table 3. Typical results are shown in figure 13. Cross coupling between injected and noninjected pins was apparent. An example, shown in figure 13, shows that although pin 6 was being driven by the input pulse, coupling to pin 10 occurred.

**Table 3. 25-pin F-type characterization**

| Insertion frequency (MHz) | Insertion loss | | |
|---|---|---|---|
| | Measured before (dB) | Measured after (dB) | From manufacturer specifications (dB) |
| 0.04 | 0.05 | 0.06 | Not given |
| 1.54 | 0.29 | 0.89 | Not given |
| 3.20 | 2.70 | 0.72 | 3 |
| 10.00 | 3.60 | 3.62 | 5 |
| 20.00 | 10.70 | 4.37 | 9 |
| 25.00 | 14.80 | 11.10 | Not given |
| 30.00 | 18.80 | 14.43 | Not given |
| 46.50 | 30.20 | 24.03 | Not given |
| 50.00 | 35.00 | 25.80 | 15 |
| 55.00 | 35.50 | 27.20 | Not given |
| 60.00 | 38.10 | 28.30 | Not given |
| 65.00 | 40.80 | 29.00 | Not given |
| 71.50 | 43.80 | 29.87 | Not given |
| 78.00 | 46.50 | 29.47 | Not given |
| 90.00 | 50.90 | 40.80 | Not given |
| 100.00 | 53.60 | 42.87 | 25 |
| 200.00 | 64.70 | 68.53 | 43 |
| 450.00 | 79.30 | 75.60 | Not given |
| 500.00 | 82.25 | 82.32 | 65 |
| 1000.00 | 85.40 | 83.50 | 70 |

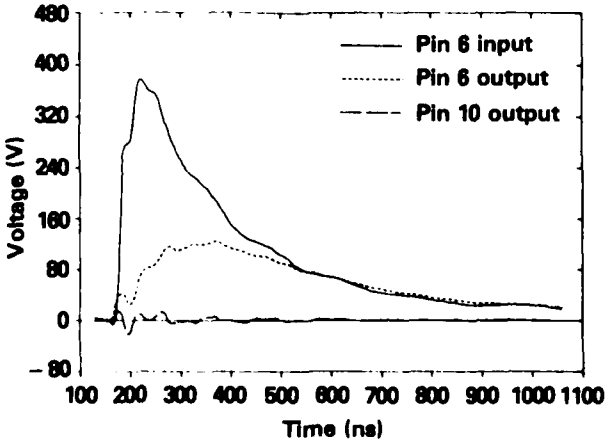



**Figure 13. F-type connector sample voltages.**

## 5.3 Gas Tube

The gas tube investigation identified characteristic voltages, currents, and transition times for the 230-84PM spark-gap surge arrestors. The characterizations were based upon exciting the surge arrestors to non-threat-level pulses, with waveshapes specified by both QSTAG-126 and MIL-STD-2169. Results indicated that the selected surge arrestor would perform well within this standard HEMP environment. However, manufacturer's specifications outlined in the data sheet provided with the surge arrestor board contain test conditions and excitation waveform parameters that are not HEMP relatable.

Typical examples of a slow-rise-time HEMP pulse (about 100 ns) and its voltage and current responses are shown in figures 14 and 15.

When excited by a fast-rise-time pulse (typically about 10 ns), the device had a transition time—the interval between the arrival of the applied signal and the moment when the device ignites (or arcs)—between 20 and 40 ns. This can be observed from both figures 16 and 17. Also shown in figure 17 is the device's relatively wide arc region (typically about 60 to 80 ns). Figure 17 compares the voltage response of the 230-84PM arrestor to that of a comparable surge arrestor, the 350-78PM.

Table 4 summarizes the recorded characteristics for the 230-84PM surge arrestors.

## 5.4 TPD Architecture

The TPD architecture investigation was a nondestructive evaluation of the TPD circuit, including spark gaps and TransZorbs, to identify the characteristic peak voltages, transition times, and cross coupling

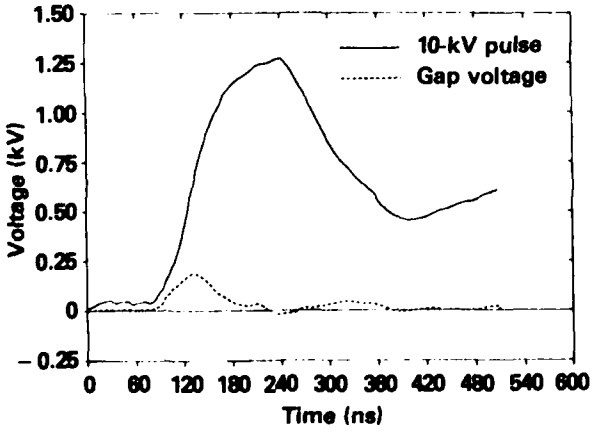



Figure 14. 10-kV pulse versus spark-gap voltage.

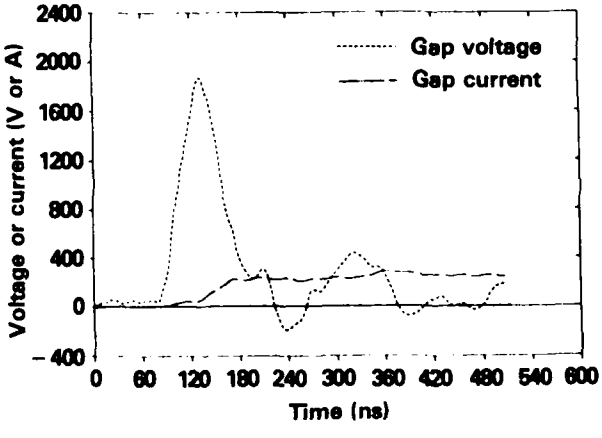



Figure 15. Spark-gap voltage versus current.

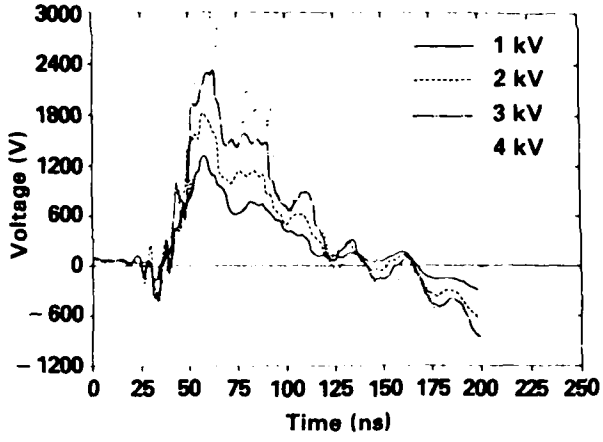



Figure 16. Spark-gap response to fast-rise variable input.

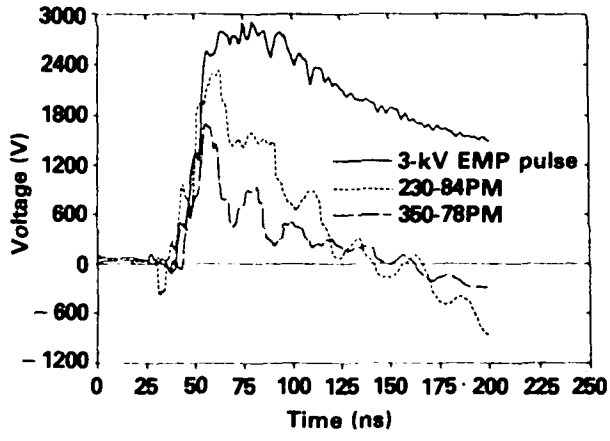



Figure 17. 230-84 PM spark gap versus 350-78PM voltage response.

Table 4. Spark-gap characteristic values

| Pulser setting (kV) | Rise time (10–90%) (ns) | Average maximum current (A) | Average breakdown voltage (kV) | Range of breakdown voltage (kV) | Average turnon time (ns) | Average turnon current (A) | Range of turnon current (A) |
|---|---|---|---|---|---|---|---|
| 1 | 11 | 67.5 | 1.1 | 1–1.2 | 19.7 | 23.6 | 17–29 |
| 2 | 12 | 124.8 | 1.5 | 1.4–1.7 | 24.1 | 66.7 | 52–71 |
| 3 | 11 | 194.8 | 2.9 | 2.8–3.0 | 17.5 | 87.8 | 82–94 |
| 4 | 13 | 280.5 | 2.8 | 2.6–3.0 | 22.3 | 112 | 96–117 |
| 10 | 77 | 279.7 | 1.7 | 1.7–1.8 | 35.0 | 54.8 | 49–59 |

at the output connectors. Since the actions of filters are sometimes detrimental to the responses of protective circuits that include TransZorbs, the F-type connector response was compared to that of an ordinary D-type connector.

A double-exponential pulse, with a rise time of 70 to 80 ns and an average peak voltage of 5 kV, was used to evaluate individual TPD circuits. Average surge-arrestor voltages were found to be 1.1 kV; based upon the results of earlier tests (shown in table 4), this was expected. Typical pulser output voltages and spark-gap responses are shown in figure 18.

Generally, results indicated that the entire TPD circuit (all three boards) could reduce the applied voltages to levels within the manufacturer's specifications, but as noted in earlier tests, well past the delay time stated. Further results indicate that both the GZ74416B 40-kb/s high-voltage board and the GZ74427A 40-kb/s low-voltage board could effectively clamp transient signals. The GZ74602B 1.54-Mb/s low-voltage board, however, could not reduce transient signals to the designed clamp voltage.

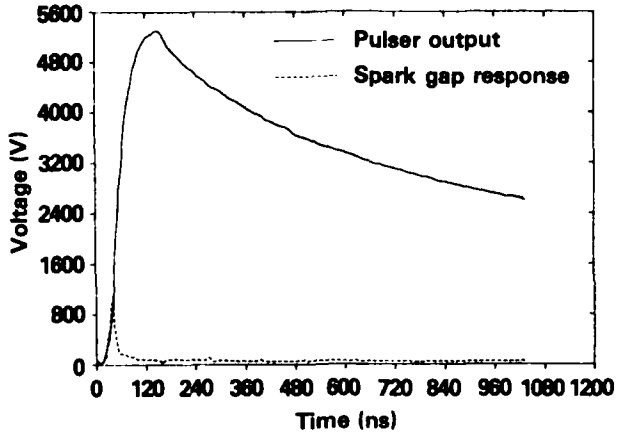



**Figure 18. Typical pulser and spark-gap voltages.**

On the average, the GZ74427A clamped voltage levels to 11 V. The average transient voltage was 19 V and the average duration was 7 μs, well within the expected limits of the circuit. The TPD circuits had similar responses with either the F-type connector or a D-type connector.

The GZ74602B board did not perform as well as expected. Clamping voltages of about 9 V were achieved; however, the average transient overshoot was 19 V. The specified clamping voltage for the board was 11.2 V maximum. The average pulse duration was 7 μs and no difference in pulse duration or peak amplitude was observed with either connector installed (F-type or D-type).

With the introduction of the GZ74416B 40-kb/s 175-V board into the TPD circuit, the action of the F-type connector became apparent for the first time (see fig. 19 and 20). It is doubtful, however, whether the F-type connector added any HEMP protection. In tests of this TPD circuit, the average maximum output voltage was 170 V. Replacing the F-type connector with a D-type connector resulted in an average output voltage of 250 V. Both voltage levels were below the 328 V specified by the manufacturer. The average pulse duration was 3 μs for both connectors. Typical output voltage responses for F-type and D-type connectors are shown in figures 19 and 20, respectively.

As noted in earlier filter pin connector tests, cross coupling was apparent, which may create upset problems in connected equipment. Therefore, output responses at both the D- and F-type connector were monitored for cross coupling.

All three boards responded to this phenomenon in similar fashion regardless of the connector. Both low-voltage boards (GZ74427A and GZ74602B) exhibited average peak-to-peak voltages of 13 V. The 175-V board, however, had average peak-to-peak levels of 35 V. Cross coupling typically lasted from 1 to 6 μs.

Typical cross-coupling responses for both F-type and D-type connectors are as shown in figures 21 and 22, respectively.

## 5.5 Data Rate Evaluation

Bit error rate testing (BERT) is done by sending a known bit sequence through the circuits within the TPD package, comparing the received bit sequence at the output of the terminal block with the known one, and analyzing the results. The bit error rate (BER) is the probability of not receiving a proper bit. BER is expressed in terms of the number of errors $\times 10^{-n}$ or in a percentage.

The SG-1139/G BERT is designed as a data-transmission system test set for two major Army systems: the Army Tactical Communication System (ATACS) and the TRITAC system. It was used in this case to simulate data transmission through the prototype TPD enclosure.

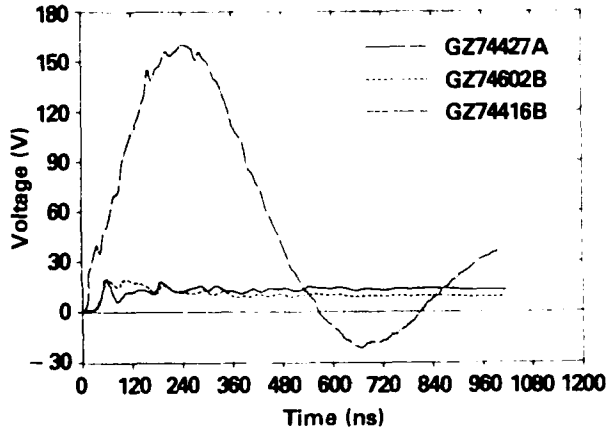



Figure 19. Typical output voltage with F-type connector.

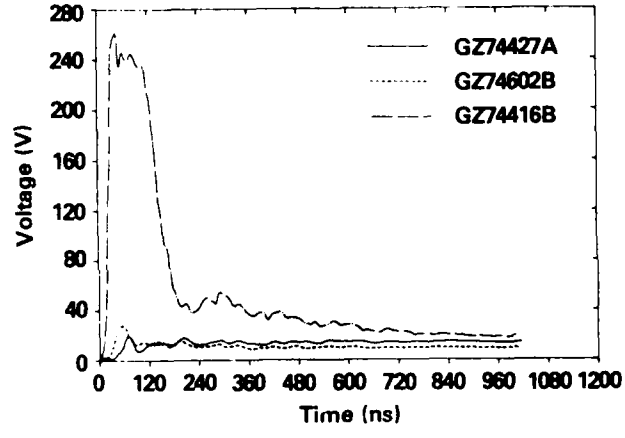



Figure 20. Typical output voltage with D-type connector.

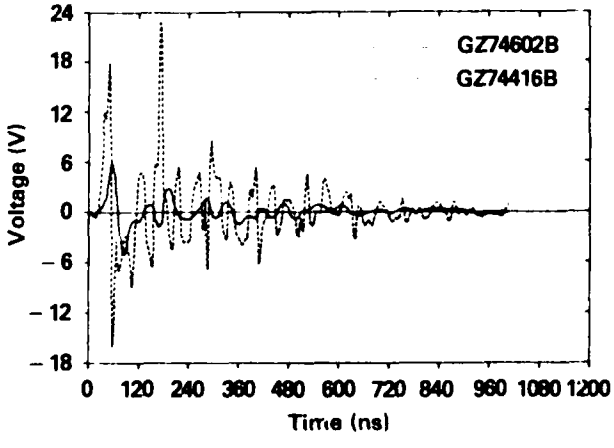



Figure 21. Typical cross-coupling voltage with F-type connector.

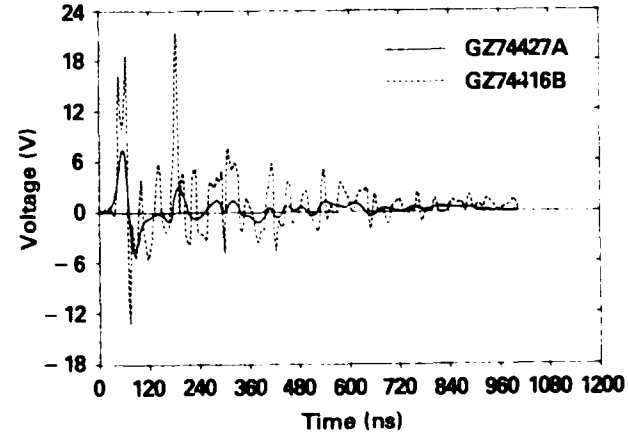



Figure 22. Typical cross-coupling voltage with D-type connector.

The three boards supplied with the TPD enclosure were installed in the enclosure and tested. Various pin pairs were selected at random. Signals up to and including 32 kb/s were injected through the cables and TPD circuits. No errors were encountered.

# 6. Design Evaluation

## 6.1 Summary

All PC boards (GZ74416B, GZ74602B, and GZ74427A) functioned within design specifications; however, peak voltage levels at the output terminal block were considered to be undesirable.

The GZ74602B 1.5-Mb/s PC board consistently allowed transient voltage overshoots that exceeded clamping voltage specifications. The F-type connector was identified to be responsible for these large transients and generally degraded the overall circuit performance.

The two low-voltage PC boards (GZ74602B and GZ74427A) are extremely susceptible to voltage cross coupling. In addition, the cable harness routing and associated geometry are not effective. Ground buses for unused data wires cannot be properly located in compartment 2.

Single TPD circuits (spark gap and TransZorb) withstood up to 4500 A for 5 μs with no observable damage.

## 6.2 Present Architecture

The purpose of the nondestructive evaluation of the present architecture was to characterize the responses of the TPD's mounted in the shielded enclosure.

The areas of principal concern in this effort were threefold: (1) to characterize the response of the TPD circuits at the terminal block output; (2) to assess the usage of both the D-type and the F-type connectors at the interface to the "clean" compartment, and (3) to quantify transient coupling in the cable routing scheme employed within the enclosure.

Transient signatures produced by varying input cable lengths were addressed by applying several transient pulse signatures using the different pulse generators. It was concluded that the greatest area of concern was with short cable lengths producing fast-rise transients. Therefore, the pulse generators were either directly connected to the enclosure or were connected to the short cable lengths at hand.

In preparation for testing, the PC boards were installed in the enclosure with filtered connectors, the output of each circuit under test was terminated with 300 Ω at the terminal block, doors were secured with a torque of 15 ft-lb, and a 5-kV signal was applied to preselected wires.

The worst-case circuit condition was achieved when the circuits not under test were left unterminated.

The surge arrestor peak voltage, when measured on the GZ74416A board, averaged 750 V on the data lines being pulsed. However, the relative position of the surge arrestor board also generated transients that were typically 700 V. Examples of these voltage levels are shown in figure 23; the appendix includes an illustration of the HDL fixture that lowered transient levels by 50 percent.

Generally, the TransZorbs performed within specifications. Voltage overshoots measured at the terminal block, however, exceeded the rated clamping voltages of the TransZorb boards. Also, the voltage level of cross coupling, in most cases, was 100 percent larger than the levels recorded in the HDL test fixture.

As designed, the PC boards clamped voltages to well below maximum specifications: the 18-V GZ74427A typically clamped to 15 V; the 11.2-V GZ74602B clamped to 10 V; and the 328-V GZ74416B clamped to 148 V. Example waveforms are shown in figure 24.

Peak voltage levels were measured and compared to each board's clamping level specifications and were as follows: the 18-V GZ74427A level was 100 percent larger and the 11.2-V GZ74602B, 250 percent larger; the 328-V GZ74416B was the exception—50 percent smaller.

At the terminal block output, voltage cross coupling was apparent. Voltage levels at terminals not connected to the pulsed TPD circuit were on the same order of magnitude as those at terminals that were connected to the circuits. These latter terminals when excited had, on the average, slightly higher maximum peak voltage levels. For in-

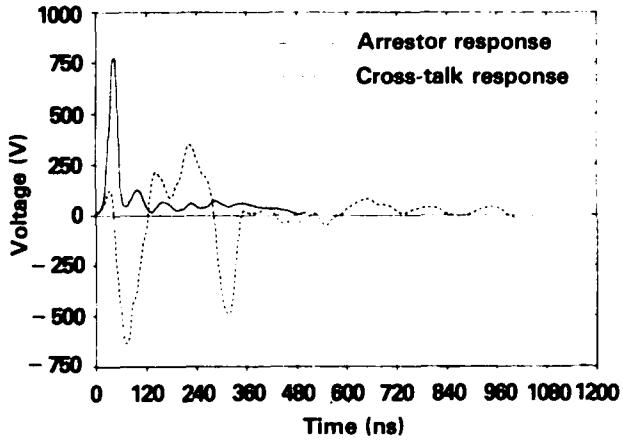



Figure 23. Surge arrestor voltage levels inside TPD enclosure.

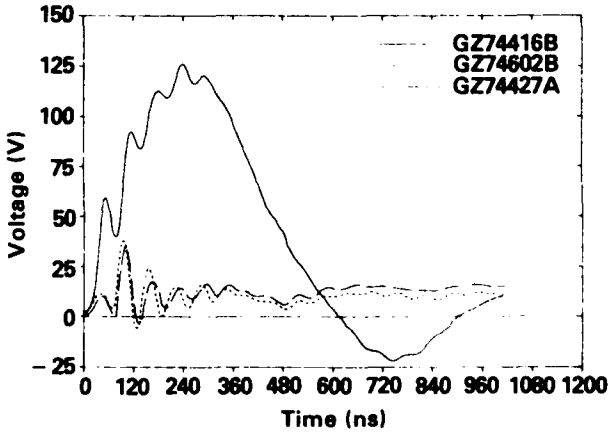



Figure 24. Typical output voltages inside enclosure.

stance, the clamping voltage of the 18-V GZ74427A was 120 percent larger than specified, and that of the 11.2-V GZ74602B was 300 percent larger. The 328-V GZ74416B, again the exception, had peak voltage levels 80 percent smaller than the PC board's specified clamping voltage. Typical examples of the voltage cross coupling at the terminal block are shown in figure 25.

Because of earlier results indicating that the F-type connector degrades the TPD circuit performance, a D-type connector was substituted for the F-type connector. With this circuit modification, the overall performance of the TPD circuits improved.

All PC boards clamped voltage levels to specifications. However, the 18-V GZ74427A and the 328-V GZ74416B had marked improvements over the performance of the circuits that included the F-type connector. Both PC boards' peak voltage levels were only 30 percent larger than the clamping voltage specifications. Performance of the 11.2-V GZ74602B also improved, allowing an increase of only 110 percent. Typical waveforms are shown in figure 26.

Additionally, peak cross-coupling voltages were also smaller. Greatest improvements occurred with the 18-V GZ74427A and the 11.2-V GZ74602B: the 18-V GZ74427A had clamping voltages 22 percent larger than specified; for the 11.2-V GZ74602B, there was an 110-percent increase over the specified clamping voltage. The 328-V GZ74416B also exhibited a small improvement. Typical waveforms are shown in figure 27. However, if these results are compared to data obtained using the HDL test fixture, they suggest that the TPD enclosure's characteristics may be further enhanced by shielding the TransZorbs from the spark gaps. As an example of the different results

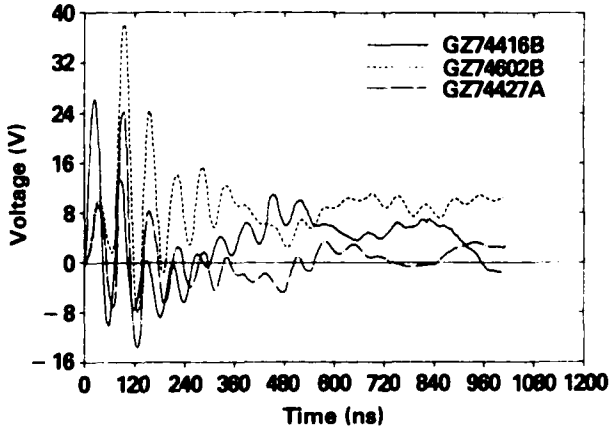



Figure 25. Typical cross-coupling voltages inside enclosure.

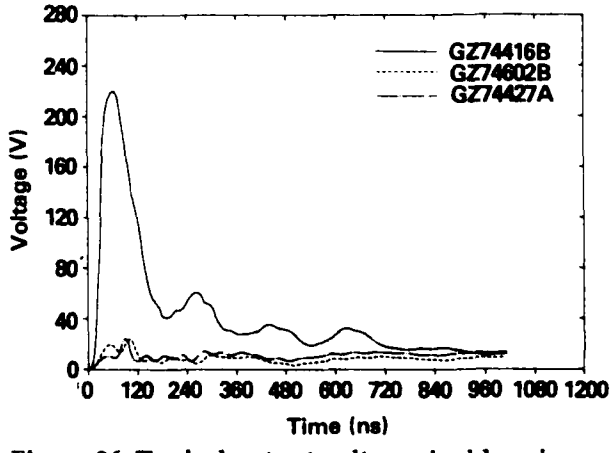



Figure 26. Typical output voltages inside using a D-type connector.

obtained using the TPD enclosure, for the 18-V GZ74427A, the voltage was 60 percent larger; for the 11.2-V GZ74602B, it was 80 percent larger; and for the 328-V GZ74416B, it was 7 percent larger than the board voltage clamping levels.

Average data for these three PC boards are summarized in tables 5 to 7.

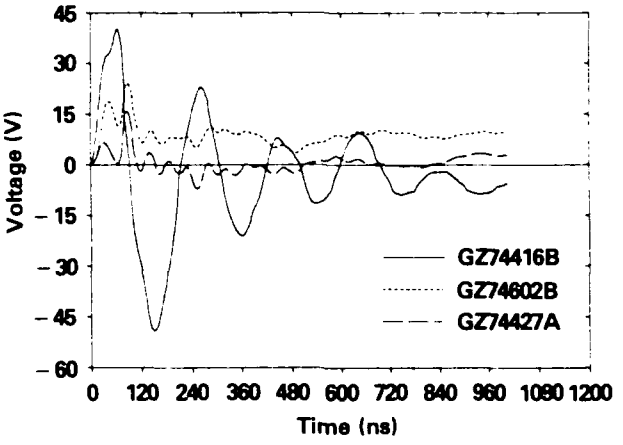



**Figure 27. Typical cross coupling inside using a D-type connector.**

**Table 5. GZ74427A performance summary**

| Configuration | | Load | | | Cross coupling | | |
|---|---|---|---|---|---|---|---|
| | | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% |
| Prototype enclosure: | with F-type | 38.6 | 15.0 | 6 µs | 37.8 | * | 600 ns |
| | without F-type | 24.3 | 13.0 | 6 µs | 22.3 | 6.4 | 2 µs |
| HDL test fixture: | with F-type | 19.0 | 14.5 | 6 µs | 14.7 | * | 1 µs |
| | without F-type | 18.2 | 14.1 | 6 µs | 12.2 | * | 600 ns |

*Indeterminate

**Table 6. GZ74602B performance summary**

| Configuration | | Load | | | Cross coupling | | |
|---|---|---|---|---|---|---|---|
| | | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% |
| Prototype enclosure: | with F-type | 43.8 | 10.0 | 6 µs | 46.0 | 10.0 | 6 µs |
| | without F-type | 24.0 | 10.0 | 6 µs | 24.0 | 10.0 | 6 µs |
| HDL test fixture: | with F-type | 18.5 | 8.5 | 6 µs | 10.8 | * | 1 µs |
| | without F-type | 27.6 | 8.5 | 6 µs | 17.5 | 12.5 | 400 ns |

*Indeterminate

Current measurements were made within the dirty compartments 1 and 2 to identify currents into the ground buses and to ascertain F-type and D-type connector characteristics.

Data wires terminating at the compartment 1 ground bus carried 240 A. Those wires terminating at the compartment 2 ground bus carried 45 A. The remaining current is shunted to the compartment 1 ground bus via the surge arrestor. Examples are shown in figure 28.

Measuring the currents on the cable harness between the surge suppressor board and the PC boards verified that the F-type connector's performance degrades the TPD enclosure's characteristics: the maximum degradation for the D-type connector occurred at 45 A; the maximum for the F-type connector occurred at 55 A. Typical current responses are shown in figure 29.

**Table 7. GZ74416B performance summary**

| Configuration | | Load | | | Cross coupling | | |
|---|---|---|---|---|---|---|---|
| | | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% | Maximum voltage (V) | Clamping voltage (V) | Pulse width 50–50% |
| Prototype enclosure: | with F-type | 148.0 | * | 1.5 µs | 36.4 | * | 1 µs |
| | without F-type | 220.0 | 50.0 | 2 µs | 89.4 | 89.4 | 700 ns |
| HDL test fixture: | with F-type | 182.0 | * | 1 µs | 39.0 | * | 700 ns |
| | without F-type | 264.0 | 220.0 | 200 ns | 34.7 | 34.7 | 400 ns |

*Indeterminate

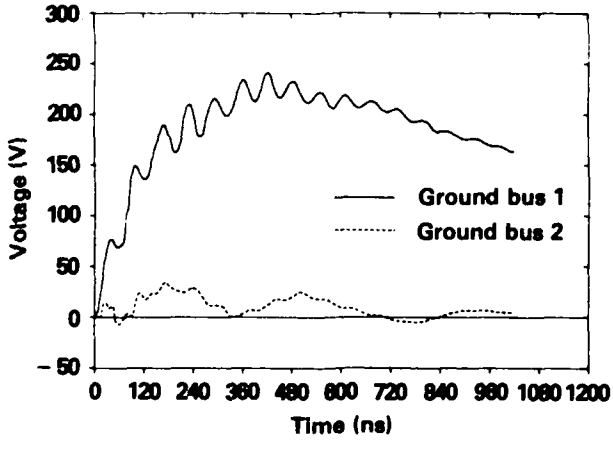



Figure 28. Typical current responses at ground buses.

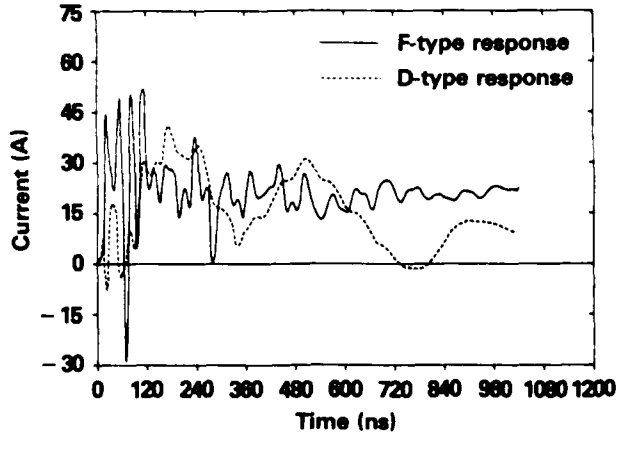



Figure 29. F-type and D-type current responses.

## 6.3 Current Injection

The intent was to impress large currents through the TPD circuits, mounted in the prototype enclosure, to the point where the circuitry was damaged. However, because of a lack of knowledge of how the enclosure was to be used and of previous test results, testing was conducted to only a limited extent.

Using the HDL power line pulser, peak currents up to a total of 6500 A were injected into the enclosure through the data wires, connected together, and through the TPD circuits; peak current levels for a single driven wire were 4500 A. Unusually high load currents and load voltages (across 300 Ω) were observed at the terminal block.

Initially, single TPD circuits were excited by increasing the pulser output voltage in 1-kV steps. Current measurements were made at these three locations: (1) the cable bundle entering the TPD enclosure near the stuffing tube, (2) the wire harness connecting the surge arrestor board and the TransZorb board, and (3) the terminal block. Figure 30 shows the peak current levels measured entering the enclosure and close to the surge arrestor board for low, medium, and high current ranges from the pulser. The maximum current measured there was 4500 A.

An additional surge arrestor characteristic was obtained from this testing: the surge arrestor impedance. Analysis based upon the pulser's internal impedance and the measured current level of the surge arrestor indicated that the impedance of the surge arrestor is 1.2 (±0.03) Ω. Figure 31 displays this information.

Bulk currents on the cable harness (between the surge arrestor to the PC boards) were typically 70 to 80 A. Load currents and voltages at the terminal block were as shown in figure 32.

Periodically, the PC boards were removed to check surge arrestor and TransZorb characteristics using the curve tracer. No degradation to either component was detected.

A final test included bulk current injection: All data wires were joined together and connected to the pulser. A separate cable, used as a ground return, was terminated at the ground bus in compartment 1. Internal access was through a waveguide (installed by HDL). In this

test configuration (shown in fig. A-9, in the appendix), the maximum current delivered to the circuitry was 6500 A (measured on the entrance cable bundle).

Other current levels measured were PC board cable harness (130 A) and terminal block load currents (40 A).

Both surge arrestor and TransZorb characteristics were again checked using the curve tracer. No degradation to either component nor to the ground paths was observed.

No further current injection was performed for the following reasons: (1) the surge arrestor breakdown voltages were determined to be abnormally high based upon the observed results from this and previous tests, (2) load currents were high and tended to increase with the injected current, and (3) the system intended to be linked to the prototype enclosure was unknown.

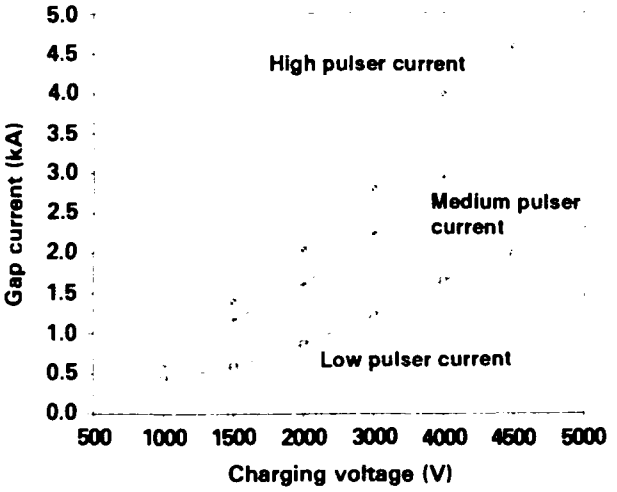



Figure 30. High-level current-injection characteristics.

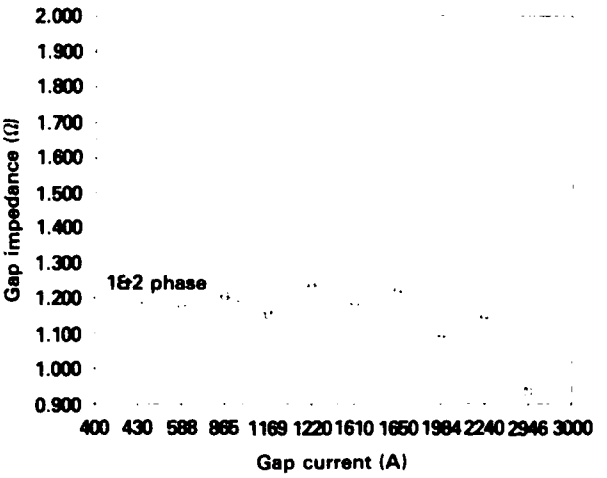
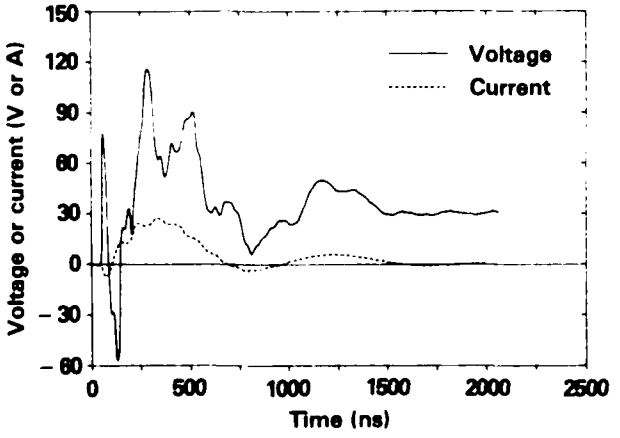



Figure 31. Spark-gap impedance.

Figure 32. Load characteristics.



# 7. Conclusion

The development and design of HEMP hardening devices and enclosures is, at best, a complex task. Solutions must relate and integrate favorably with the unit and the system to be hardened without affecting either the overall performance of the system or any other hardening concern, such as TEMPEST, RFI/EMI, and EMC. The evaluation of this brassboard TPD enclosure is a prime example of such a task.

The evaluation encompassed many areas of hardening concerns. Some key areas for improvement were identified:

a. SE for the enclosure can improve, provided suggested modifications to the enclosure cabinetry are implemented.

b. Transient suppression is, at best, marginal. One TPD board performed within specifications and need not be modified. The remaining two PC boards require more stringent manufacturing specifications and probable component replacement.

c. The 25-pin F-type connector must be replaced.

d. The present circuit architecture (that is, the methods by which the TPD boards are installed, including the associated wiring) must be changed.

It is recommended that a redesign of the enclosure based upon the presented suggestions will improve the performance and satisfy standard hardening requirements.

# Appendix —Test Equipment and Procedures

## Appendix

### CONTENTS

## FIGURES

# A-1. Baseline/Degradation SE Test

## A-1.1 Test Equipment

The equipment required for the baseline/degradation shielding effectiveness (SE) test is as follows:

TS-450 Shielded Enclosure Test Set

- 450-MHz transmitter unit
- 450-MHz receiving unit
- 20-ft coaxial cable
- Dipole antennas
- Battery charging unit
- Charging cables
- System carrying case

Torque wrench

## A-1.2 Test Procedures

The test procedures used to characterize the baseline shielding effectiveness and to assess life-cycle degradation include the following tasks:

### *A-1.2.1 450-MHz Shielded Enclosure Test Set Calibration*

1. Position the 450-MHz receiver and transmitter in a configuration for calibrating the system.
2. Activate both the transmitter and receiver by turning the power switches to the on position and check the battery conditions; then deactivate both units. If either unit indicates a battery condition insufficient for operation of the unit, charge the batteries.
3. Connect the 20-ft extension cable and antenna to the receiver unit.
4. Attach the second antenna to the transmitter unit and place the unit inside the TPD enclosure section to be tested (clean or dirty section).
5. Before calibrating the system, place the receiver dipole antenna approximately 5 ft from and parallel to the transmitter antenna. To calibrate the system, set the zero set control on the receiver to the fully counterclockwise position and set the attenuation range switch to 0 dB. Activate both the receiver and transmitter units and adjust the receiver zero set control for a 0-dB reading on the attenuation meter.

During this process, be careful to keep the path between the receive and transmitter antennas clear of any reflecting objects.

### *A-1.2.2 Baseline Shielding Effectiveness Test*

The TS-450 calibration (see sect. A-1.2.1) should be completed before the baseline SE test is performed. The TPD enclosure has three compartments; the test configurations for these compartments are shown in figures A-1 to A-3.

1. Activate the 450-MHz transmitter unit and place it in the clean side (protected from high-altitude electromagnetic pulse (HEMP)) of the enclosure.

2. Close the enclosure door and tighten the fastening bolts starting from the top left, then proceed to the bottom right, top right, and bottom left. Then alternate the tightening of the middle fasteners. This tightening procedure should provide a uniform bonding of the door/gasket to the outside flange area of the enclosure.

3. Activate the 450-MHz receiver, and adjust the attenuation range switch to the 80-dB setting. Place the receiving antenna approximately 2 in. from the exterior surface of the door. Start scanning the selected test locations. If an attenuation measurement is detected below 80 dB

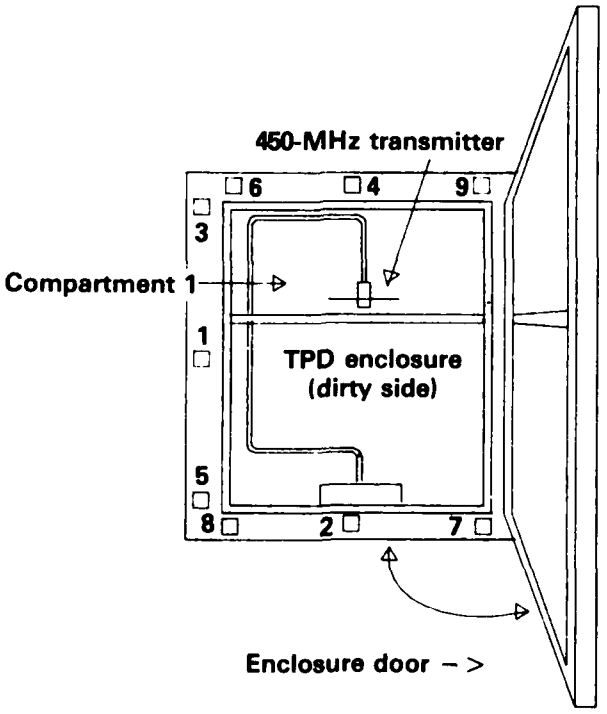



**Figure A-1. Compartment 1 baseline SE test setup.**

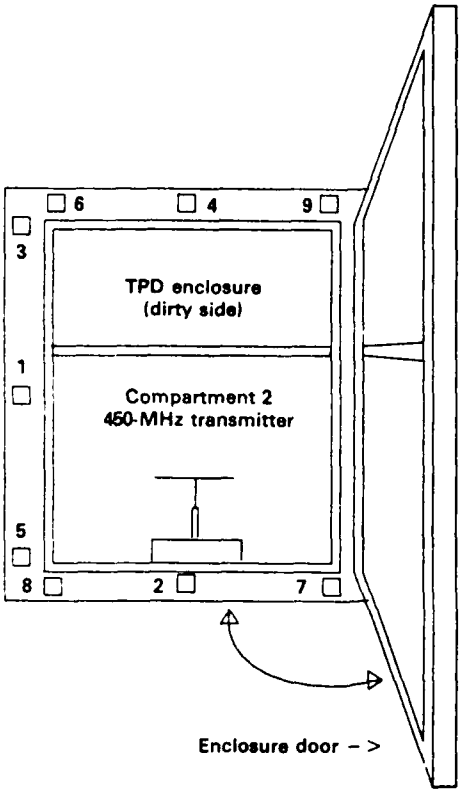



Figure A-2. Compartment 2 baseline SE test setup.

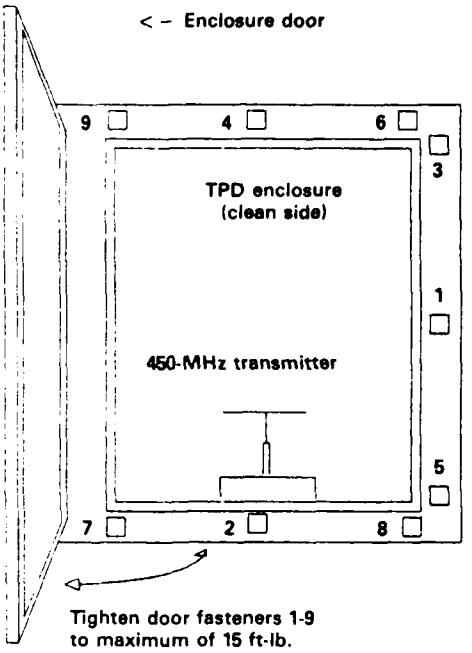



Figure A-3. Compartment 3 baseline SE test setup.

on the receiver attenuation meter, scan the area to determine the location of the highest signal level (the lowest attenuation reading, in decibels). This actual attenuation level is determined by adding the meter reading and the attenuation range switch position. For example, a 60-dB switch position and an 8-dB meter reading indicates a total attenuation of 68 dB.

4. Record the decibel attenuation and the physical location of the receive antenna in relation to the enclosure door, for each measurement.

5. Deactivate the 450-MHz receiver and open the enclosure door and deactivate the 450-MHz transmitter.

6. Repeat steps 1 through 5 for SE tests of the dirty side (unprotected from HEMP) of the enclosure.

### *A-1.2.3 HA/HM Shielding Effectiveness Degradation Test*

The TS-450 calibration (see sect. A-1.2.1) should be performed before the hardness-assurance/hardness-maintenance (HA/HM) SE degradation test.

1. Activate the 450-MHz transmitter unit in the enclosure.
2. Close the enclosure door and tighten the fastening bolts starting from the top left, then proceed to the bottom right, top right, bottom left; then alternate tightening the middle fasteners using the torque wrench.
3. During this tightening procedure and after all the fasteners have been tightened, monitor the shielding effectiveness using the 450-MHz receiver attenuation meter indication, until a maximum attenuation measurement is achieved.
4. Record both the maximum attenuation value and the torque required to achieve this attenuation value.
5. Periodically perform this task to statistically monitor the degradation of the shielding effectiveness of the door-gasket interface.

# A-2. Low-Frequency SE Test

## A-2.1 Test Equipment

The equipment required for the low-frequency SE test is as follows:

HP 141T spectrum analyzer
HP 8553B low-frequency plug-in
MFJ-815 standing wave ratio (SWR)/wattmeter
ENI-350L rf power amplifier
MGL-7A field sensors
Nanofast OP-300A transmitter/receiver
Tektronix 485 oscilloscope

## A-2.2 Low-Frequency SE Test Procedures

The following methodology was employed to assess SE of the TPD enclosure to low-frequency continuous wave (cw) illumination.

First an MGL-7A reference sensor was inserted onto the parallel plate. The sensor was connected to a 485 oscilloscope within the shielded room by double-shielded semirigid heliax cable.

The sweep oscillator was then varied from 300 kHz to 105 MHz. Using the SWR meter, it was possible to locate the frequencies at which maximum power was realized across the parallel plates. At those frequencies, field reference levels were observed on the oscilloscope and recorded.

Next, the MGL-7A data sensor was centered and elevated so as to be equidistant from both upper and lower plates. The sensor was oriented to obtain the maximum magnetic (H) field excitation. An OP-300A fiber-optic data system was used to transmit the sensor response to a spectrum analyzer located within the shielded room.

The parallel plates were then injected with the frequencies indicated in tables 1 and 2 (main body of report) and at the corresponding reference levels. Sensor output levels were observed from the spectrum analyzer and recorded.

The TPD enclosure was then positioned within the parallel plates so that the data sensor (once located within the enclosure) would be at the same relative position to the plates as it was without the enclosure present (see fig. A-4). In order to minimize cable pickup, a metal tube was used to shield the TPD cables from the radiated field.

The parallel plates were again injected with the indicated frequencies and at the respective reference levels. Sensor output levels were observed and recorded as before.

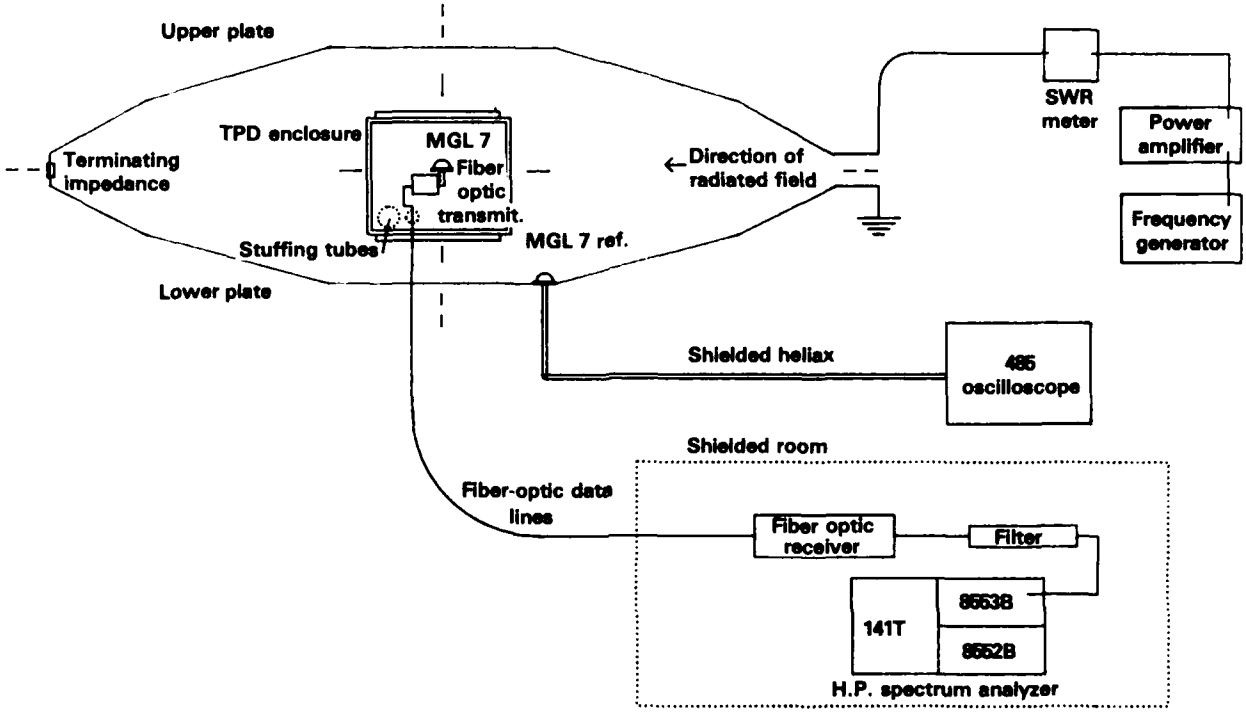



Figure A-4. Low-frequency SE assessment test setup.

# A-3. F-Type 25-Pin Connector Test

## A-3.1 Test Equipment

The equipment required for the F-type 25-pin connector test is as follows:

| | |
|---|---|
| HP 3577A | network analyzer |
| HP 8753A | network analyzer |
| Tektronix 7104 | oscilloscope |
| Tektronix 7A29 | wide-band vertical amplifier |
| Tektronix 7A16 | vertical amplifier |
| Tektronix 7B29 | horizontal time base |
| Tektronix DCS01 | digitizing camera |
| Tektronix P6015 | high-voltage probe |

## A-3.2 F-Type 25-Pin Connector Test Procedures

The 25-pin F-type connector was evaluated to (1) verify the specifications for insertion loss, (2) observe the filter response to a double-exponential pulse, and (3) observe any degradation in insertion loss due to pulse stressing.

A connector was mounted inside a shielded test fixture (shown in fig. A-5). The filter pins were loaded with 240-Ω resistors.

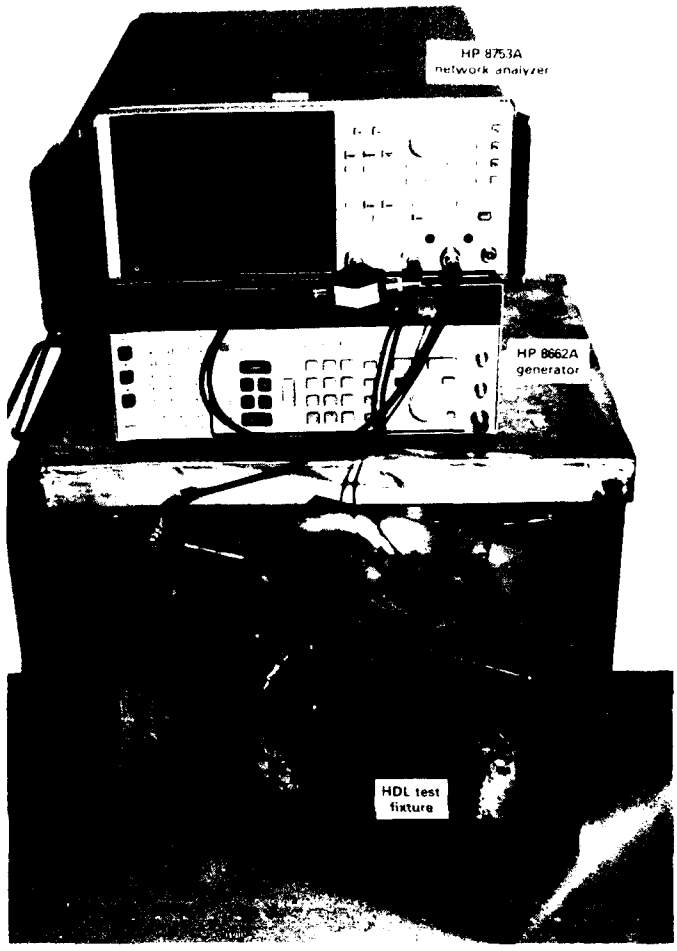
Insertion loss for three filter pins was measured from 3 MHz to 1 GHz using the network analyzers.

Three filter pins were selected for pulse testing. The pins were then consecutively energized using the HDL GC 2 pulser. The pulser's source impedance was 50 Ω.

Each pin was excited by 10 pulses. Voltage measurements were made at the output of the pin under stress and at the output of others to determine the average level of pin-to-pin voltage coupling.

The pulse injector was then disconnected and the insertion loss for the three filter pins again measured using the network analyzers.

**Figure A-5. 25-pin F-type connector characterization equipment.**



# A-4 Gas Tube Test

## A-4.1 Test Equipment

The equipment required for the gas tube test is as follows:

Tektronix 7104 oscilloscope
Tektronix 7A29 wide-band vertical amplifier
Tektronix 7A16 vertical amplifier
Tektronix 7B29 horizontal time base
Tektronix DCS01 digitizing camera
Tektronix P6015 high-voltage probe

## A-4.2 Gas Tube Test Procedures

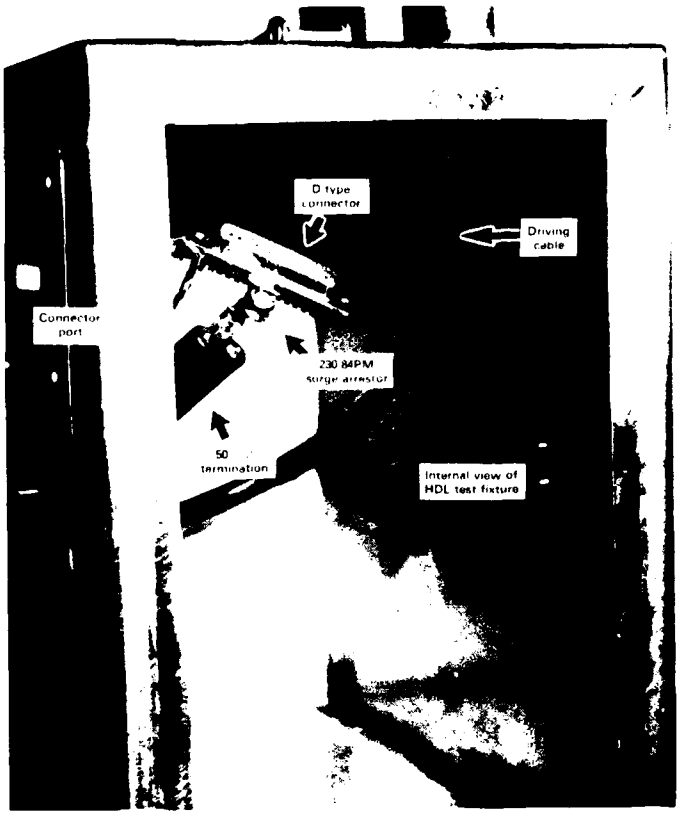
The 230-84PM surge arrestor was evaluated to determine the device's typical breakdown voltage and arc region when stressed by a double-exponential pulse.

A single 230-84PM arrestor was connected to the backshell of a D-type connector. The arrestor and connector were then mounted inside the shielded test fixture (shown in fig. A-6). Output pins on the D-type connector were loaded with 240-Ω resistors. The lid was secured and, using either the HDL GC 2 pulser or the HDL WD-1 pulser, a double-exponential pulse was applied to the arrestor. Source impedances for the pulsers were 50 Ω.

Voltage measurements were made by connecting the Tektronix 6015 high-voltage probe to the D-type connector outside the fixture and using the DCS01-supported data-acquisition system. Measurements indicated the noise floor environment to be 80 mV.

For comparison, the 350-78PM surge arrestor was put in place of the 230-84PM, and the same measurements were performed on it.

**Figure A-6. Surge arrestor with test hardware.**



# A-5. TPD Architecture Test

## A-5.1 Test Equipment

The equipment required for the TPD architecture test is as follows:

Tektronix 7104 oscilloscope
Tektronix 7A29 wide-band vertical amplifier
Tektronix 7A16 vertical amplifier
Tektronix 7B29 horizontal time base
Tektronix DCS01 digitizing camera system
Tektronix P6015 high-voltage probe
Tektronix P6006 voltage probe

## A-5.2 TPD Architecture Test Procedures

The following procedures were employed to characterize the actions of the various TPD circuit boards when used in combination with the 230-84PM surge arrestors and F-type and D-type 25-pin connectors.

In order to minimize the effects produced by the surge arrestor ignition, a small shielded enclosure was constructed. The input port to the enclosure allowed the connection of a double shielded GC 2 pulser lead. A 25-pin D-type connector was mounted to the output port. The surge arrestor was directly soldered to both the pulser lead and to the pin under excitation on one side and to the backshell of the 25-pin connector on the other. The pulser source impedance was 50 Ω. Ground return paths included the enclosure's case which was connected to the pulser return.

The input of the circuit board under test was connected to the 25-pin connector on the outside of the enclosure. To ensure good ground return, the backplane of the circuit board was connected to the enclosure case with steel braid.

The output of the circuit board was connected to the input of the F-type and D-type connector under evaluation. The output of these connectors was terminated with 240 Ω.

Pulser characterization was made using the Tektronix 6015 high-voltage probe while the pulsing unit was disconnected from the circuit, yet paralleled by 50 Ω.

Surge arrestor voltage measurements were also made using the high-voltage probe while the circuit board under test was connected.

Initially noise-level measurements were made with the voltage probes open and lying close to the circuit boards. Typical noise levels were less than 80 mV.

Output voltage measurements across the 240-Ω load resistors were made using the Tektronix 6006 10X voltage probe.

The test setup is as shown in figure A-7.

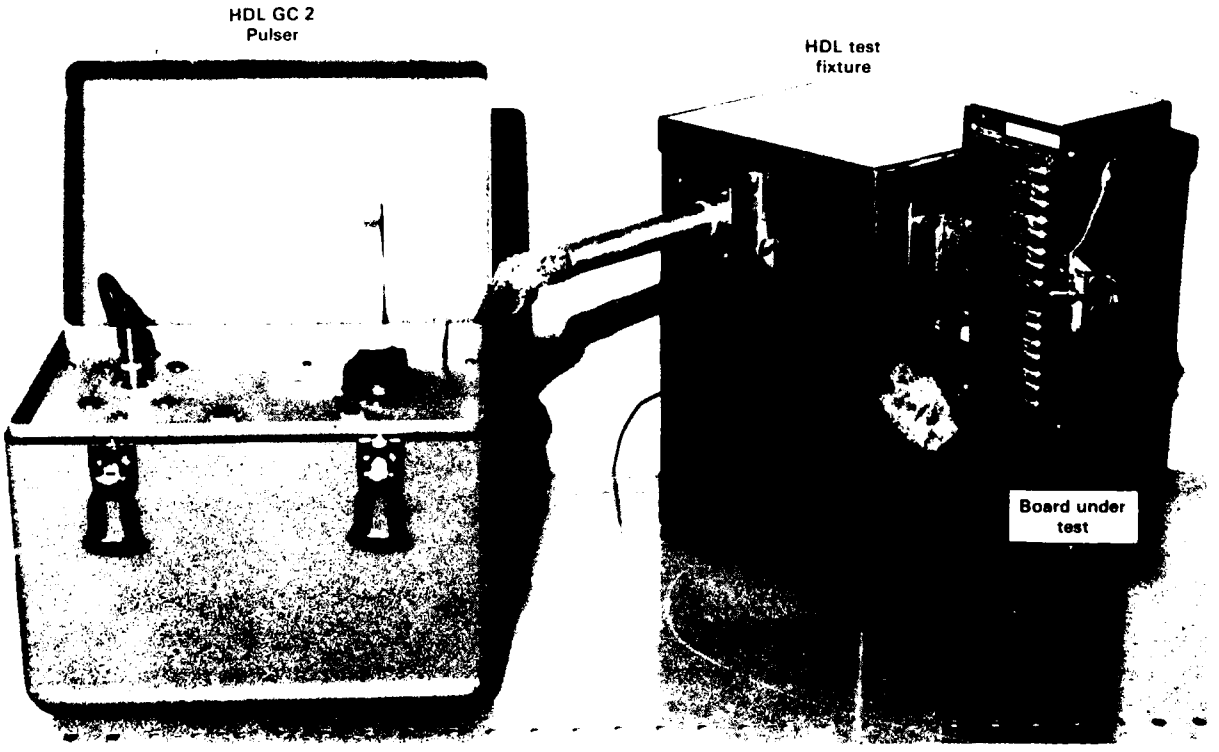



**Figure A-7. TPD circuit evaluation test setup.**

# A-6. Data Rate Evaluation Test

## A-6.1 Test Equipment

The equipment required for the data rate evaluation test is as follows:

SG-1139/G bit error rate (BER) test set
Tektronix 485 oscilloscope
Singer 93686-3 current probe

## A-6.2 Data Rate Evaluation Test Procedures

Figure A-8 is a test setup to measure the throughput of a closed-loop transmitted diphase signal containing these discrete data rates: 0.576, 0.6, 1.2, 2.4, 4.8, 9.6, and 32 kb/s.

Since the SG-1139/G is a go/no-go test set, the tester generates signal rates identified by the operator using the front panel control switches and provides output signals to the appropriate output connectors, also located on the front panel.

The signals were applied to various single wires and wire pairs selected at the input of the 10-ft signal cables supplied with the TPD enclosure. Data signals were injected into the TPD enclosure through the internal circuitry (i.e., the gas tubes, TransZorbs, and filter pin connector to the output terminal block). At the terminal block, the SG-1139/G monitored the resultant signals by interconnecting the selected wire pair to the return input of the test set.

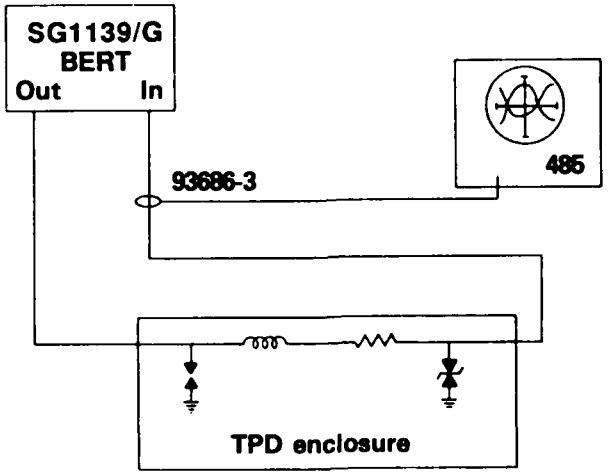



**Figure A-8. BERT setup.**

## Appendix

The BER of the system is determined using two major parameters:

(1) the amplitude of the returned signal as referenced to the signal delivered and

(2) time synchronization of the two signals.

Further analysis of the throughput signals was performed by using the oscilloscope to monitor the data passing through the TPD enclosure.

# A-7. Present Architecture Test

## A-7.1 Test Equipment

The equipment required for the present architecture test is as follows:

Tektronix 7104 oscilloscope
Tektronix 7A29 wide-band vertical amplifier
Tektronix 7A16 vertical amplifier
Tektronix 7B29 horizontal time base
Tektronix DCS01 digitizing camera system
Tektronix P6015 high-voltage probe
Singer 93686-4M current probe

## A-7.2 Present Architecture Test Procedures

The various TPD circuits were characterized within the prototype enclosure. Test procedures and methods of measurement were similar to those described in section A-5.

The GZ74427A surge-suppressor board was secured in compartment 1. The PC boards were secured, each in turn, in compartment 2. The terminal block, in compartment 3, was terminated with 300-Ω loads. Voltage and current probes were placed in the various compartments with the probe cables exiting the enclosure through the unused stuffing tubes. Both doors were closed and each fastening bolt tightened to 15 ft-lb.

The GC 2 pulser was connected to various signal cables. The return path for the pulser was connected to the cable shield. The pulser output voltage level was set to 5 kV.

Measurements were made using the DCS01 camera system to monitor voltage and current responses within the enclosure. First, these responses were measured with the PC boards connected to the terminal block via the F-type connector. Next, the PC boards were connected to the terminal block via a D-type connector. Similar measurements were made. The test setup is shown in figure A-9.


**Figure A-9. Present architecture evaluation test setup.**

# A-8. Current-Injection Test

## A-8.1 Test Equipment

The equipment required for the current-injection test is as follows:

Tektronix 7104 oscilloscope
Tektronix 7A29 wide-band vertical amplifier
Tektronix 7A16 vertical amplifier
Tektronix 7B29 horizontal time base
Tektronix DCS01 digitizing camera system
Tektronix P6015 high-voltage probe
Singer 93686-4M current probe
Singer 93686-3 current probe

## A-8.2 Current-Injection Test Procedures

Initially, single TPD circuits were excited by increasing the pulser output voltage in 1-kV steps. The pulser lead was connected directly to the surge arrestor board through the unused stuffing tube. The enclosure's doors were closed and tightened to 15 ft-lb. Current levels were monitored at the pulser output, at cables leading from the surge arrestor board to the PC boards, and across the 300-Ω load at the terminal block output. In order to increase the amount of available current to the TPD circuits, the four pulser output phases were tied together.

Next, with all four pulser outputs tied together, the cables associated with the surge arrestor board and running external to the enclosure were injected. All the wires in the two cable bundles were stripped back and soldered together with the pulser lead. The cable bundle shields were released from the stuffing tubes in order to minimize current coupling within the bundles. Other unused cables connected to the ground bus in compartment 1 were removed. A separate ground return cable was connected to the ground bus in compartment 1 and exited the enclosure through the unused stuffing tube. The circuits were again energized and similar measurements were made.

The test setup is as shown in figure A-10.


**Figure A-10. Current injection test setup.**

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